ROHITH DR

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https://github.com/Rohith-DR

OBJECTIVE

To pursue a role in the VLSI domain where I can utilize my knowledge of electronics, HDL-based design, and analytical problem-solving to work on advanced chip design and verification projects.

EXPERIENCE

Jr Research Fellow (R V college of engineering) Bat Conservation India Trust | [04-08-2025]

- Designed and implemented an IoT system based on Raspberry Pi with a client–server architecture, embedded firmware in C and Python, custom PCB design, functional prototypes, and successful field validation.
- Engineered and prototyped an ultrasonic microphone system capable of capturing bat echolocation signals from 15 kHz to beyond 180 kHz, followed by successful real-world field testing.

VSDSquadron Mini Internship Vlsi System Design | [19-01-2025]

- Designed a Shipment Tracking System in C, compiled it using PlatformIO with the RISC-V toolchain for hardware-level implementation insights.
- Engaged in a 4-week intensive research internship, focusing on the VSDSquadron Mini RISC-V development board, strengthening skills in embedded systems and processor design.

EDUCATION

Bachelor of Engineering, Electronics and Communication, GAT 2021-2025
specialization: Embedded systems & VLSI, CGPA: 9.81/10, First Rank Holder and Gold Medallist

SKILLS & ABILITIES

- **Programming Languages:** C, C++, Python, Java, HTML, JavaScript, Verilog, SystemVerilog, Embedded C, MATLAB.
- **Tools:** Arduino, RTOS, Keil µVision, Cadence Virtuoso, COMSOL Multiphysics, KiCad, ModelSim, Visual Studio Code, LTspice, MATLAB/Simulink, Vivado, Quartus Prime, PlatformIO. Icusverilog, GTKwave.
- **Soft Skills:** Communication, Teamwork, Leadership, Problem-Solving, Critical Thinking, Analytical Skills, Time Management, Adaptability, Decision-Making, Project Coordination.

PROJECTS

Binarium : 8-Bit Processor for EdTech Learning:

- Designed and simulated a microprocessor architecture in Verilog, implementing core components like the ALU, Control Unit, and Registers, and verified functionality using simulation tools.
- Prototyped and simulated the design using ModelSim with testbenches, validating instruction cycle, data flow, and bus communication for functionality and performance.

Verilog Simulation GUI (Python-based):

- Developed a Python GUI tool integrating Icarus Verilog (ICUS) and GTKWave to streamline Verilog code compilation, simulation, and waveform analysis.

Bat Signal Detector:

- Designed and simulated (LTspice) an ultrasonic microphone for bat echolocation detection across a 15 kHz–180+ kHz frequency range. validated performance through laboratory and real-world field testing.
- Developed and evaluated multiple client–server architecture prototypes, optimizing system performance and noise reduction to enable remote, long-range, high-speed data transfer.

CERTIFICATIONS

- NPTEL Certificate on Hardware Modeling Using Verilog.
- Internship Certificate from VSD
- Internship Certificate from Elewayte.
- NPTEL Certificate on Embedded System Design using ARM.
- Certificate of Merit in Circuit Designing and Simulation Hackathon (VSD), securing a Top 20 position.